

FIG. 1

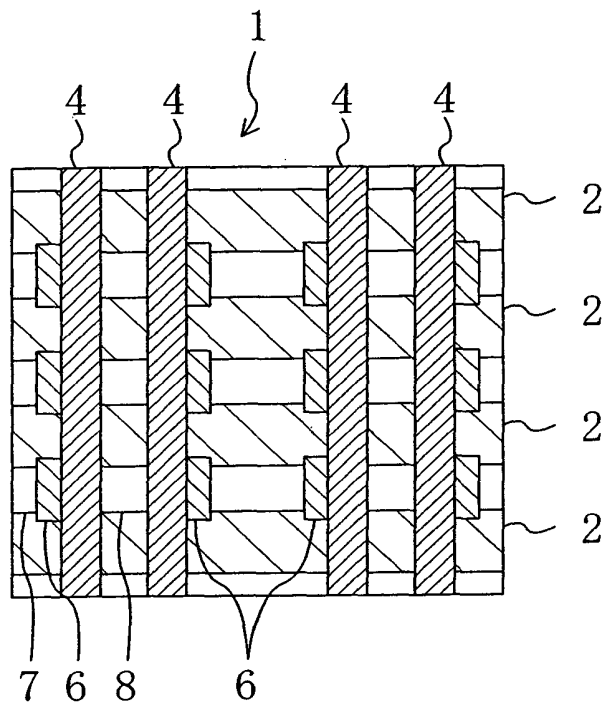


FIG. 2A

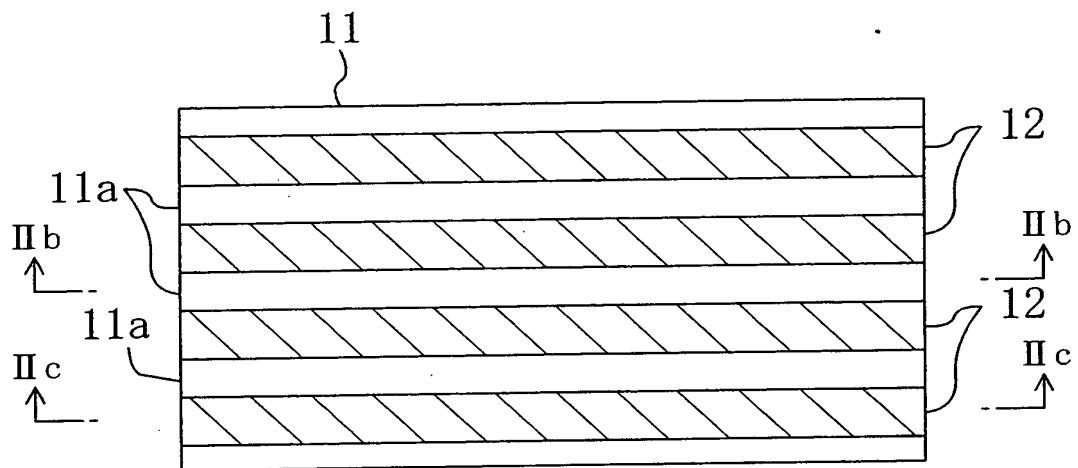


FIG. 2B

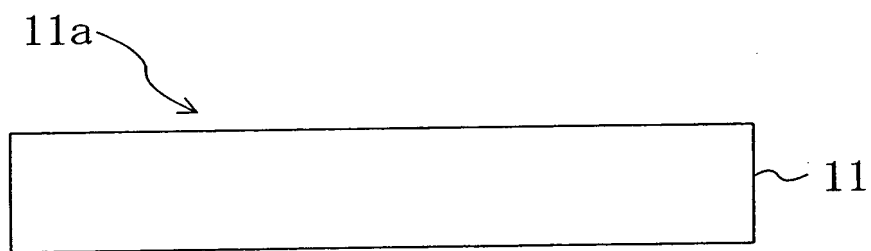
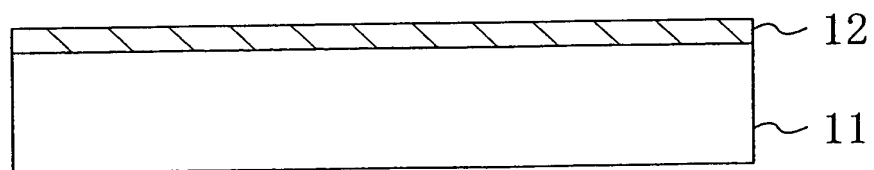


FIG. 2C



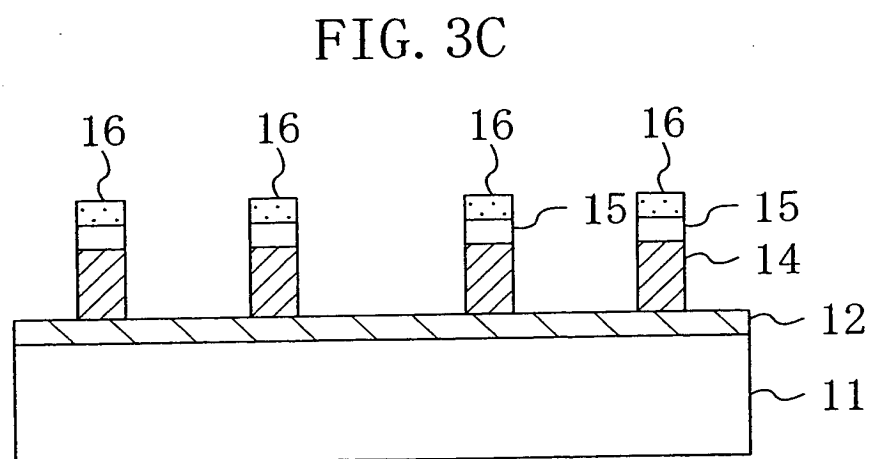
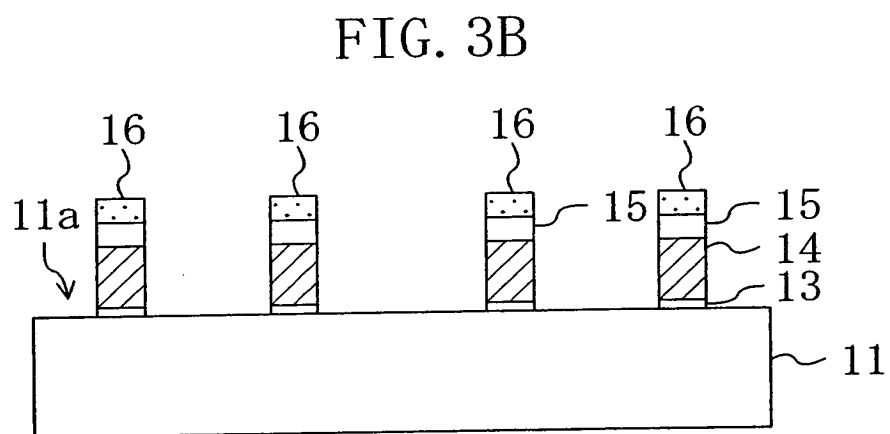
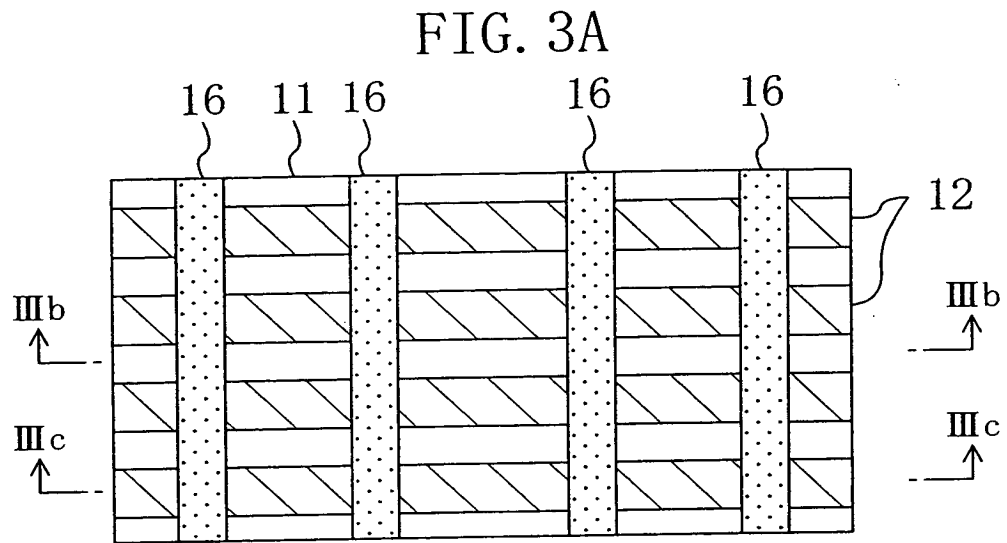


FIG. 4A

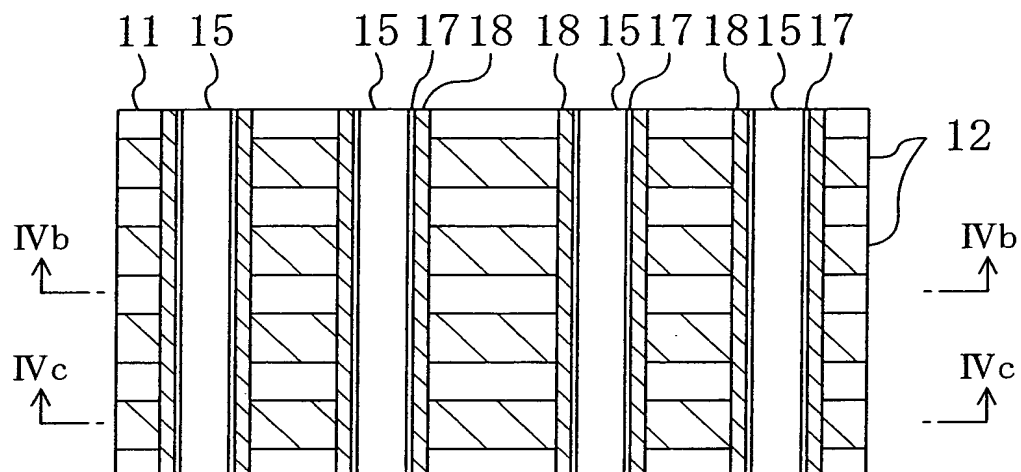


FIG. 4B

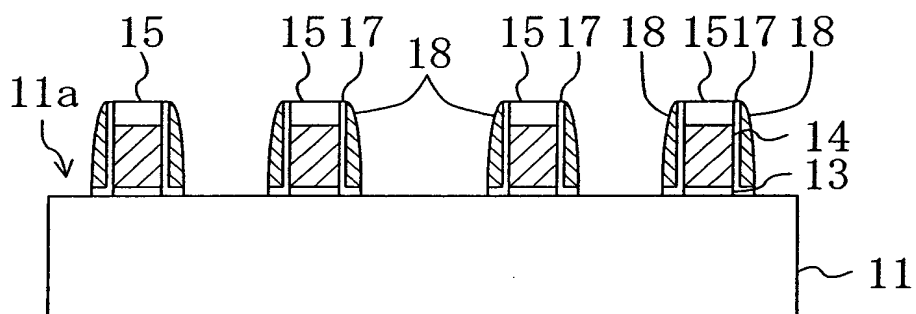


FIG. 4C

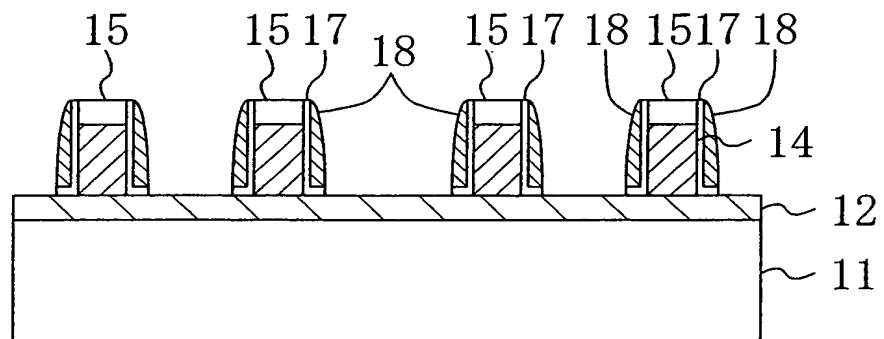


FIG. 5A

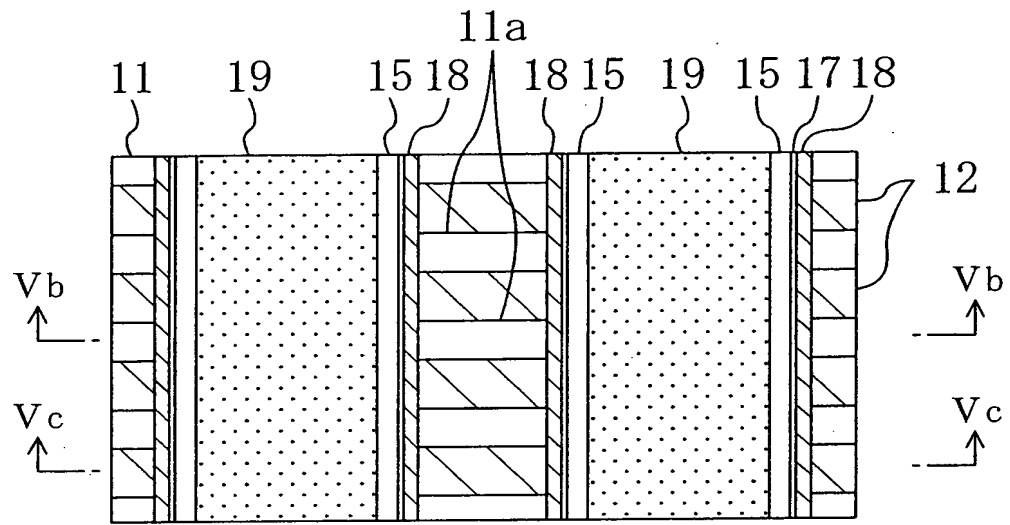


FIG. 5B

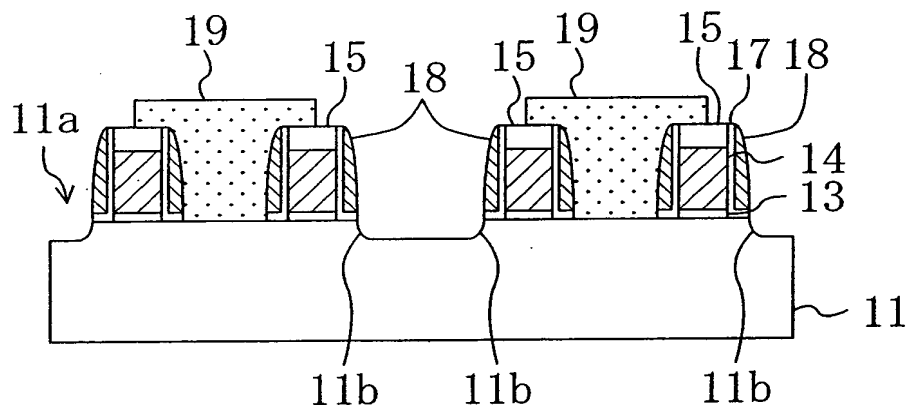
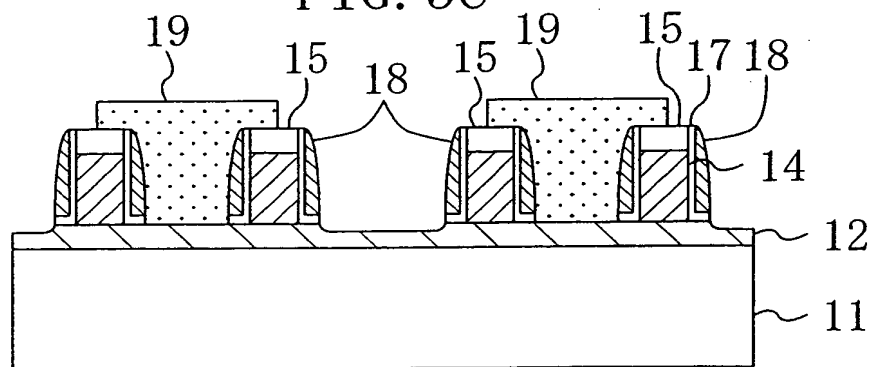


FIG. 5C



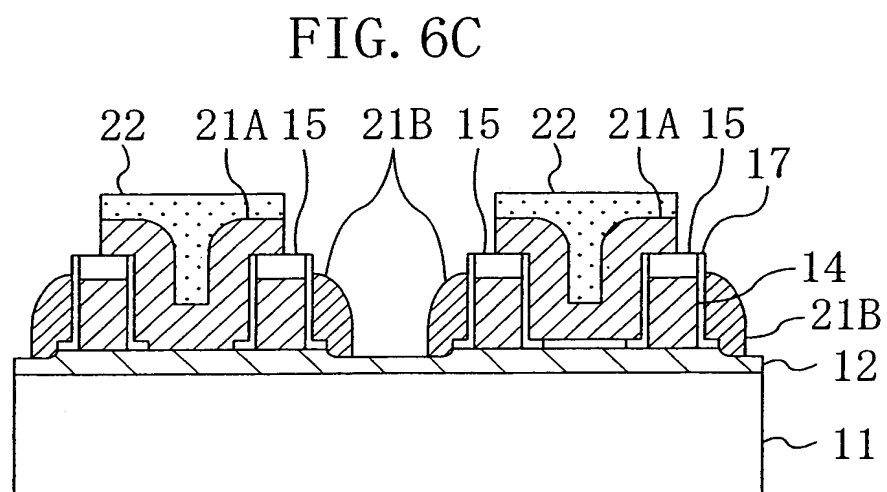
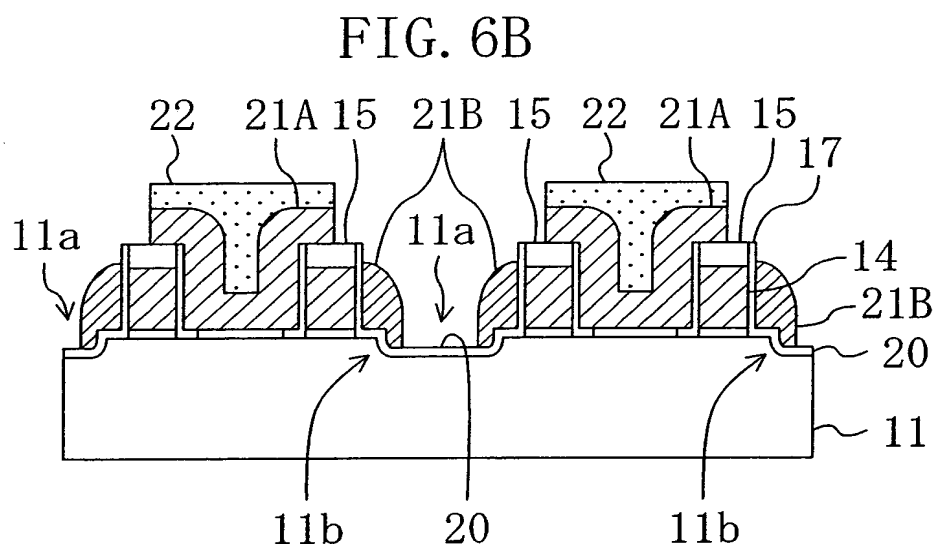
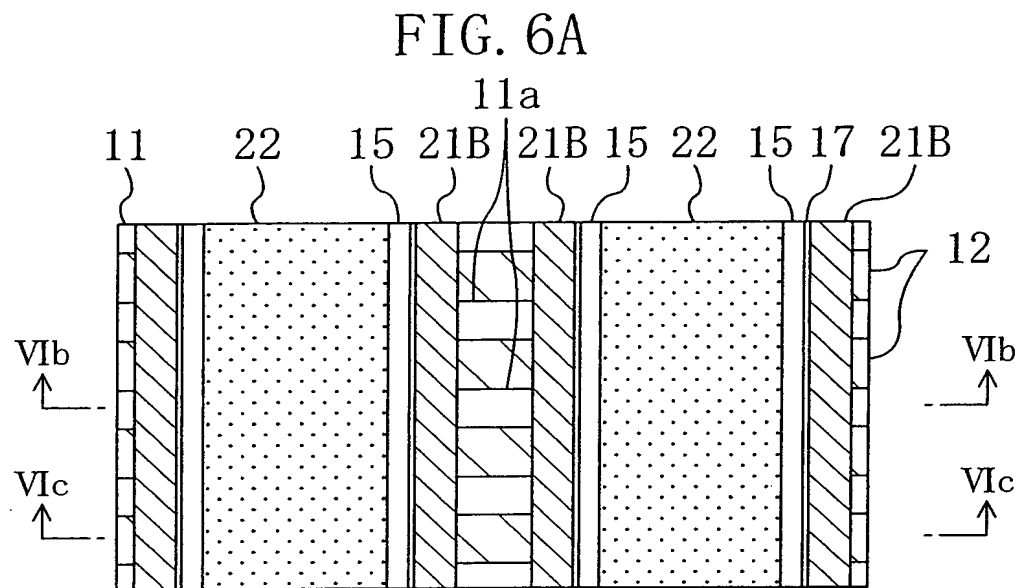


Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 11, which is divided into a top layer 11a and a bottom layer 11b. A series of rectangular structures 15 are formed on the top layer 11a, separated by a material 20. The structures 15 are covered by a layer 21, which is divided into regions 21A and 21C. A layer 23 is formed on top of the structures 15.

A cross-sectional view of a substrate 11 with a top surface 12. Four solder bumps 15 are mounted on the top surface 12. Each bump 15 consists of a solder core and a solder cap. The bumps are arranged in a row.

A cross-sectional view of a semiconductor device. The device consists of a base layer 11, a patterned layer 20, and a top layer 21C. The patterned layer 20 includes a series of rectangular blocks 14 and 15, and a central dome-shaped structure 17. The top layer 21C is a thin layer on top of the patterned layer. The device is shown in a cross-section with various layers and structures labeled with reference numerals.

A cross-sectional view of a semiconductor device. It features a substrate with a series of four pillars. Each pillar consists of a central core (hatched pattern) and an outer shell (dotted pattern). The pillars are labeled 15. The top surface of the pillars is labeled 24. The space between the pillars is labeled 17.

FIG. 9A

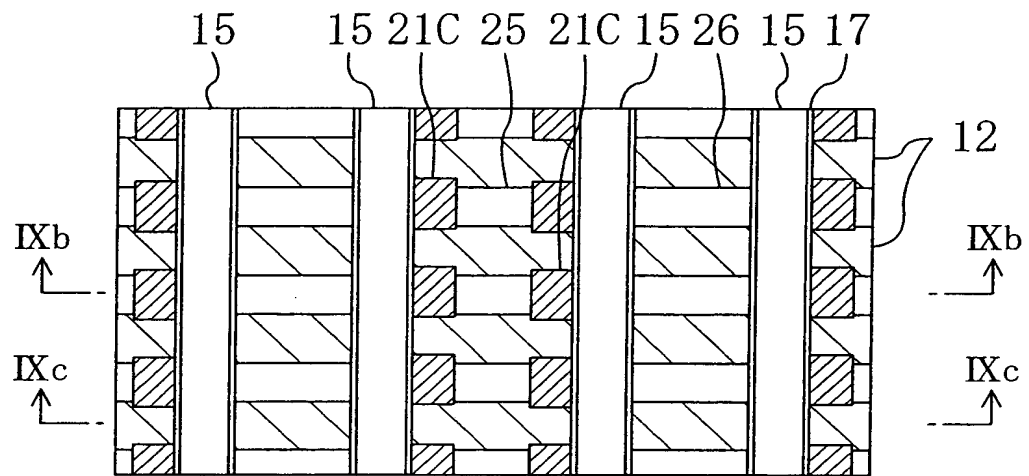


FIG. 9B

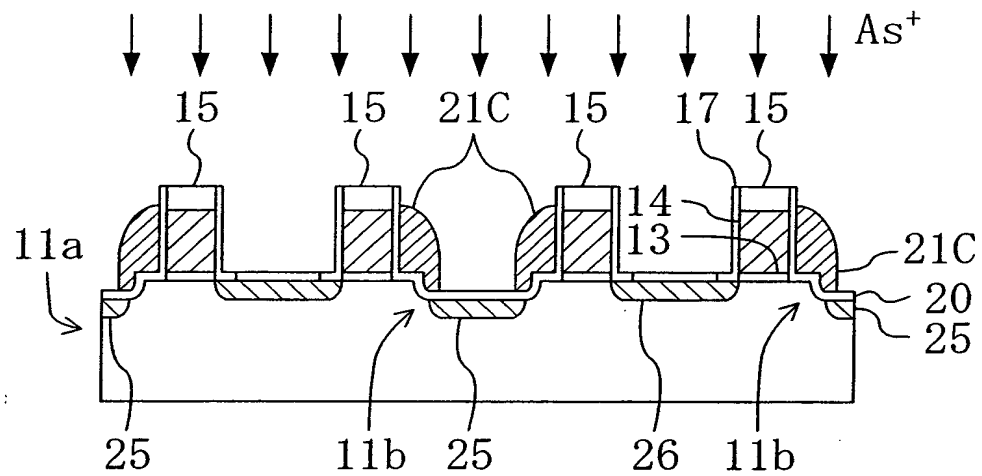


FIG. 9C

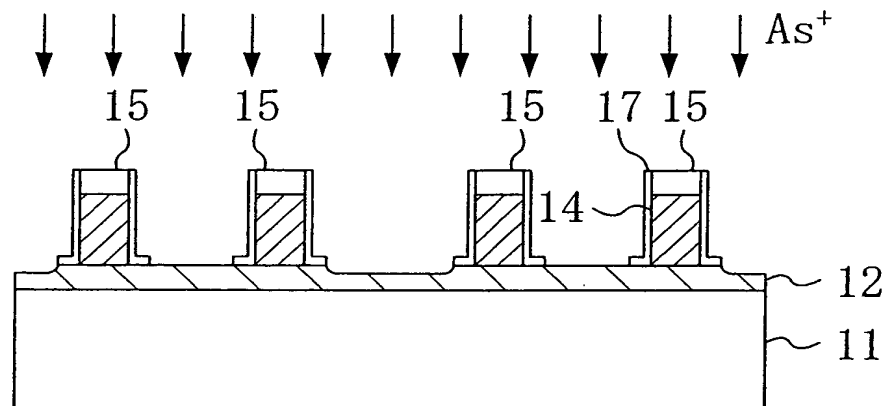


FIG. 10A

PRIOR ART

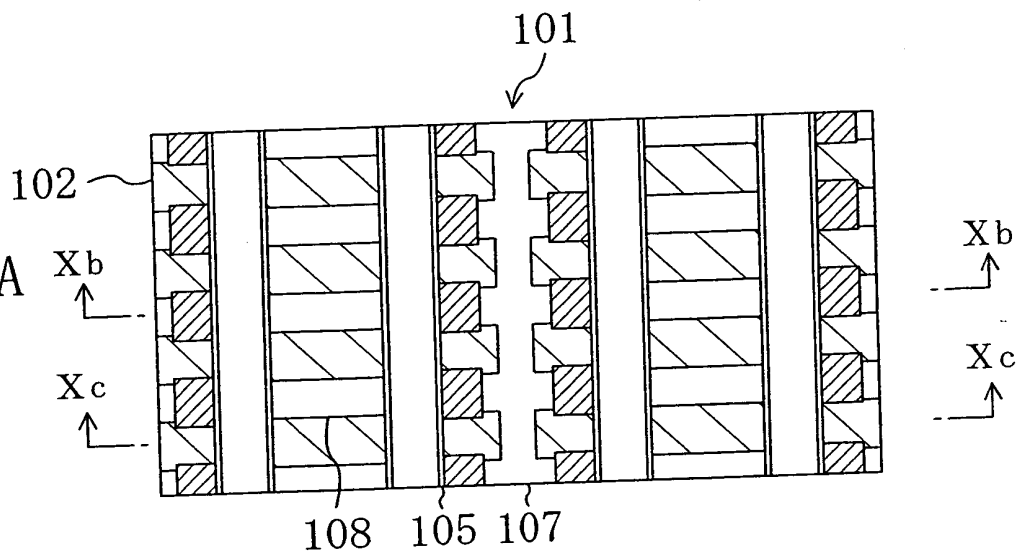


FIG. 10B

PRIOR ART

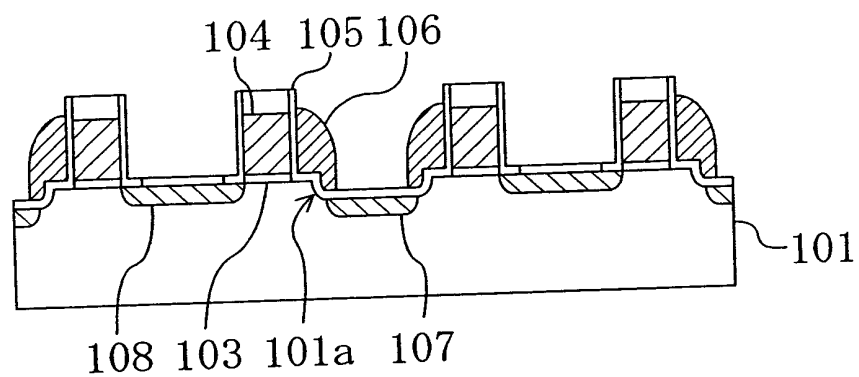


FIG. 10C

PRIOR ART

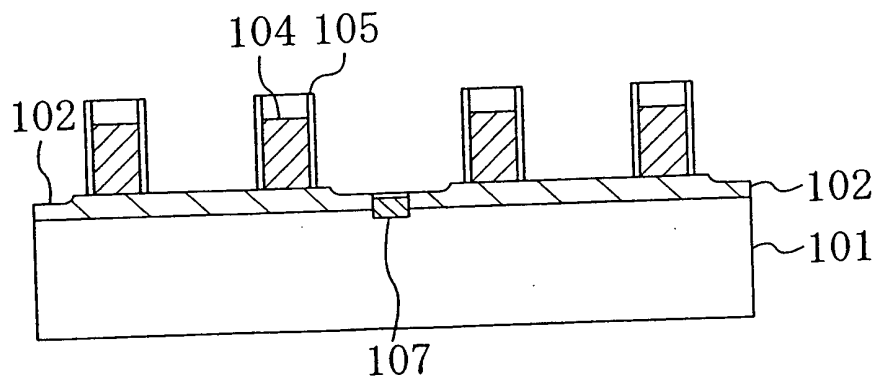


FIG. 11A

PRIOR ART

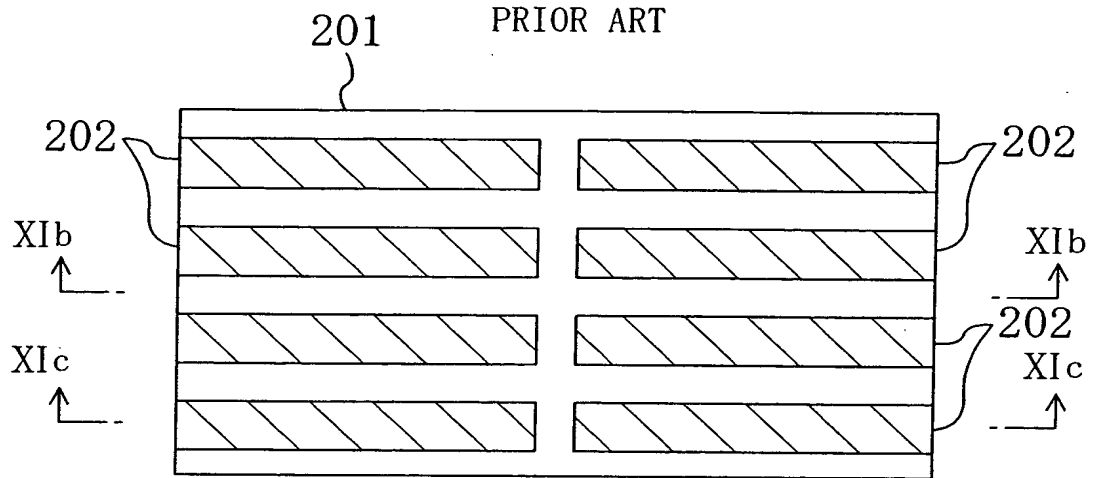


FIG. 11B

PRIOR ART

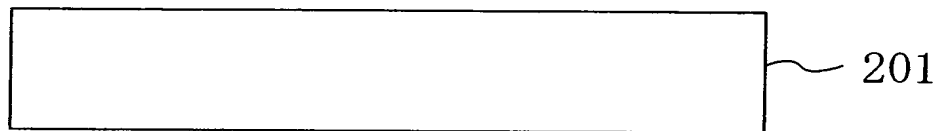


FIG. 11C

PRIOR ART

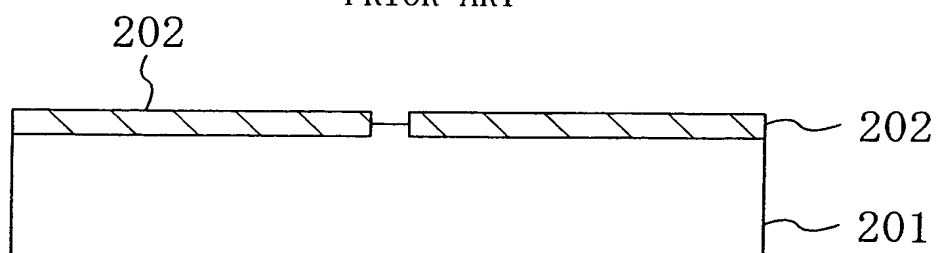


FIG. 12A

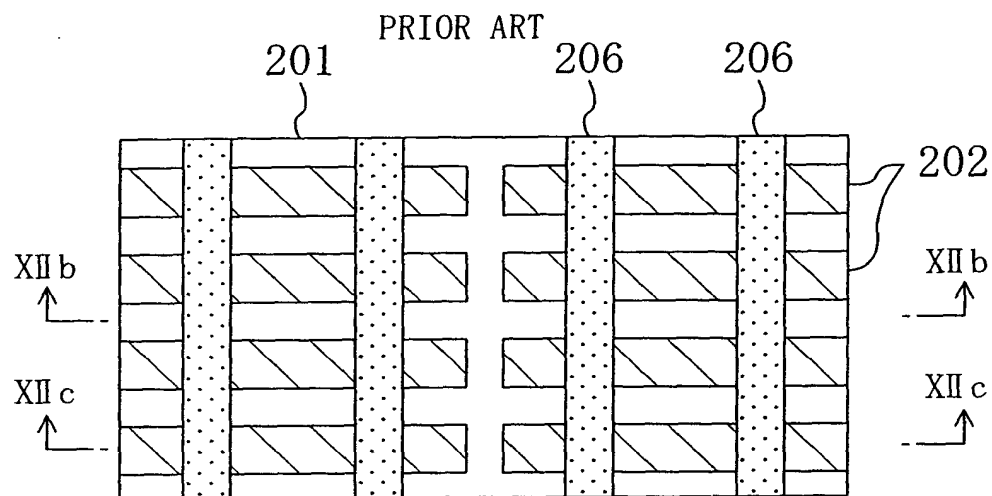


FIG. 12B

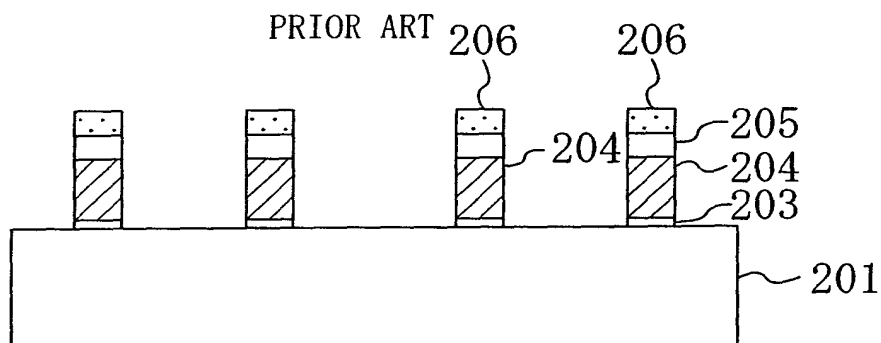


FIG. 12C

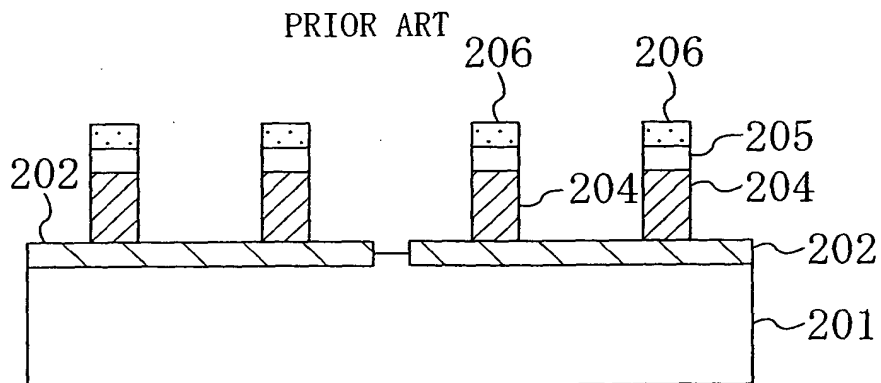


FIG. 13A

PRIOR ART

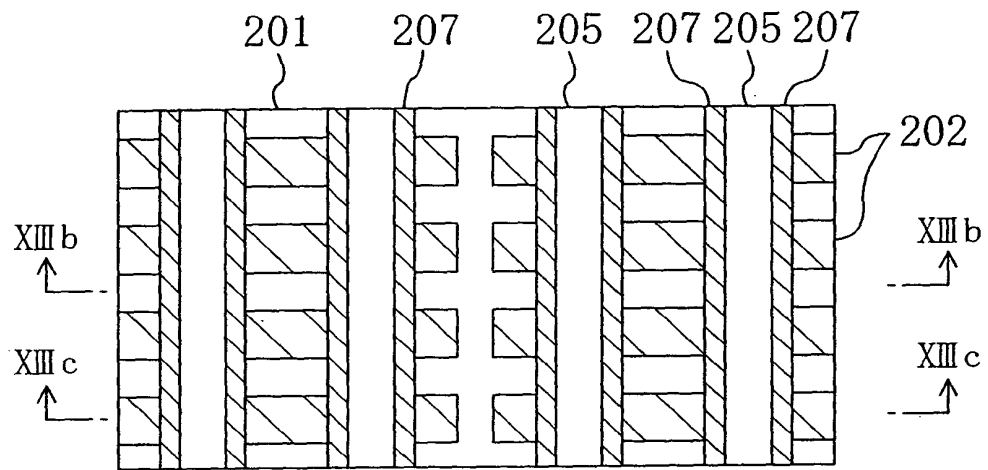


FIG. 13B

PRIOR ART

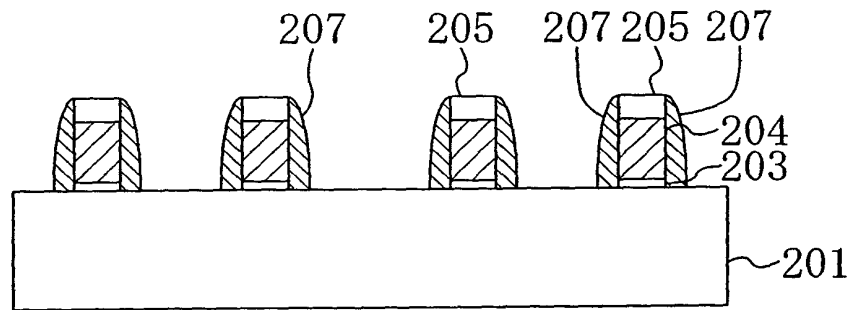


FIG. 13C

PRIOR ART

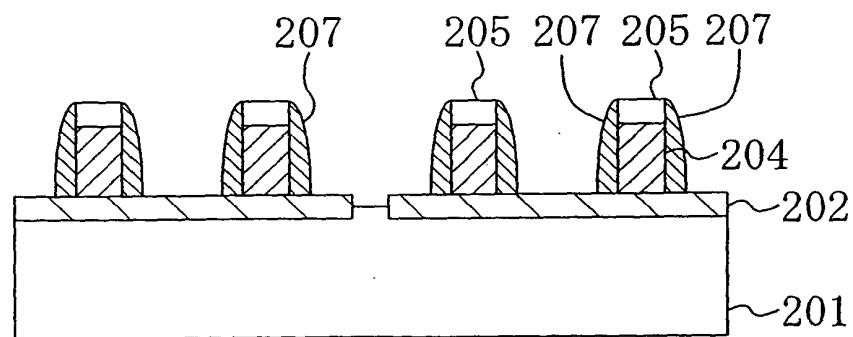


FIG. 14A

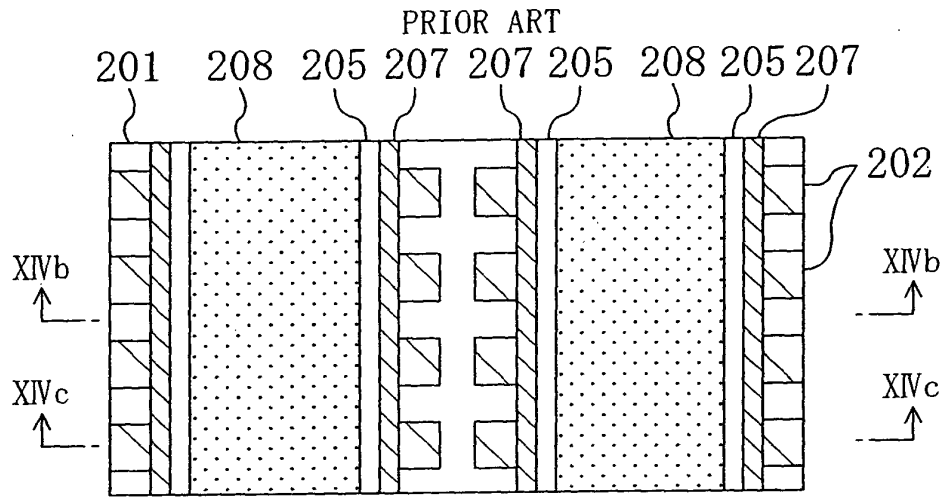


FIG. 14B

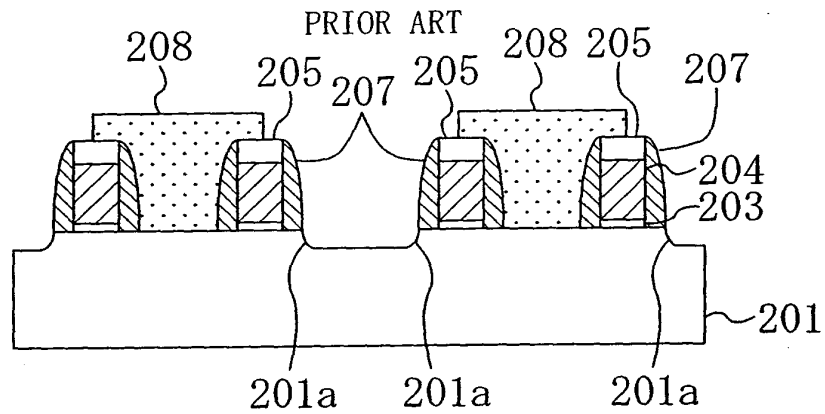
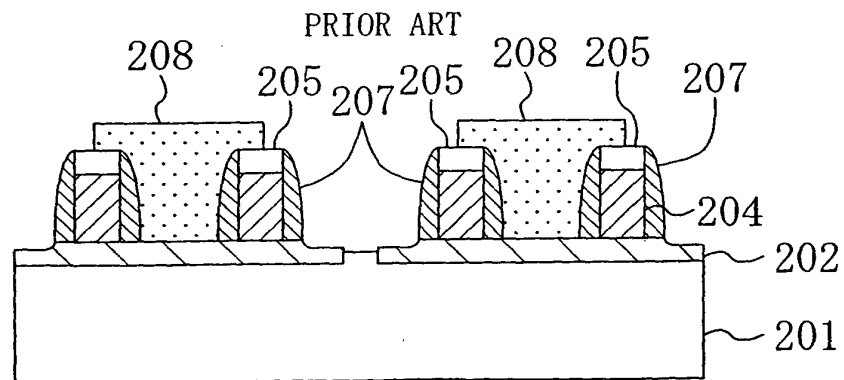
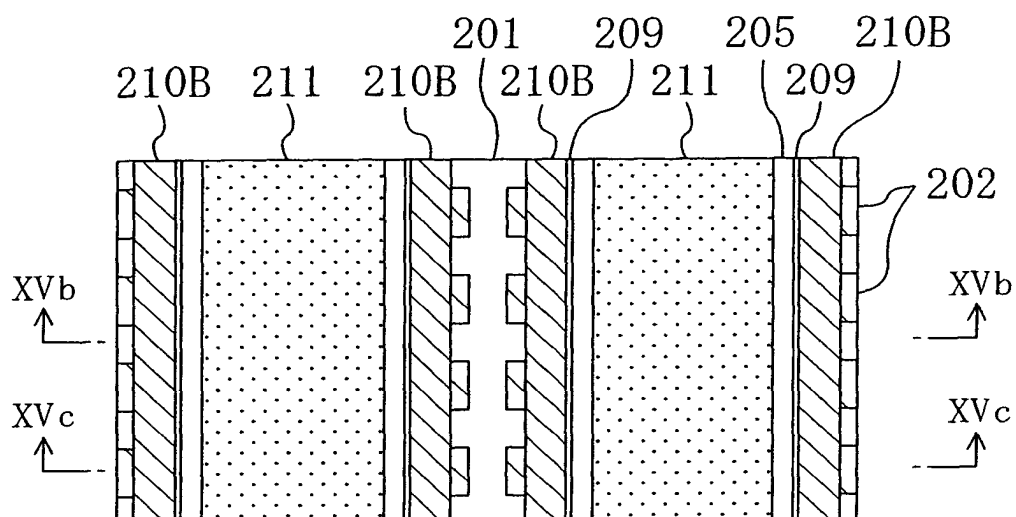


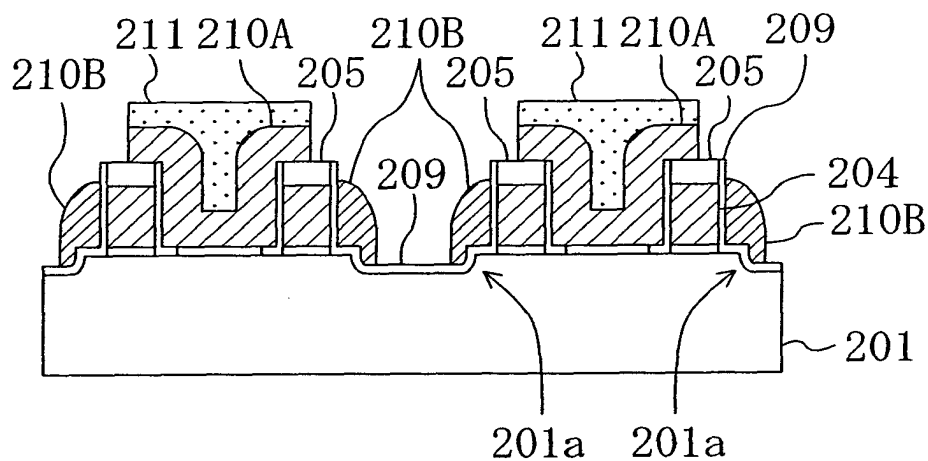
FIG. 14C



PRIOR ART



PRIOR ART



PRIOR ART

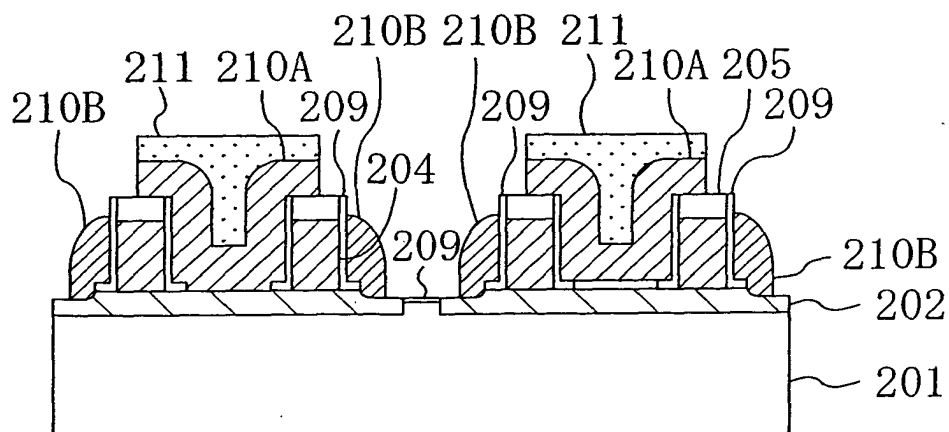


FIG. 16A

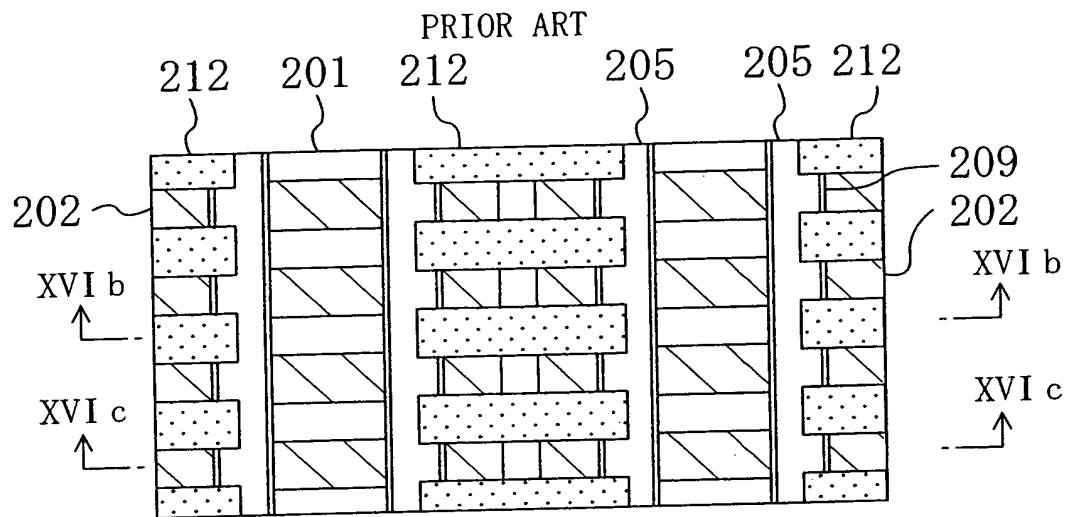


FIG. 16B

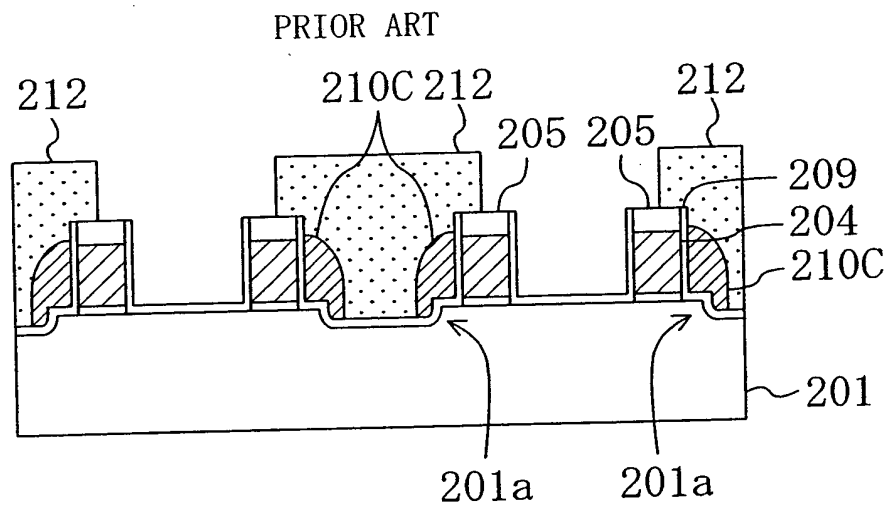
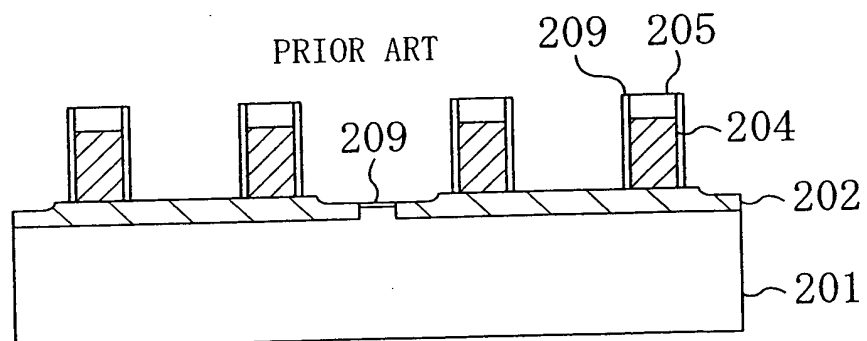


FIG. 16C



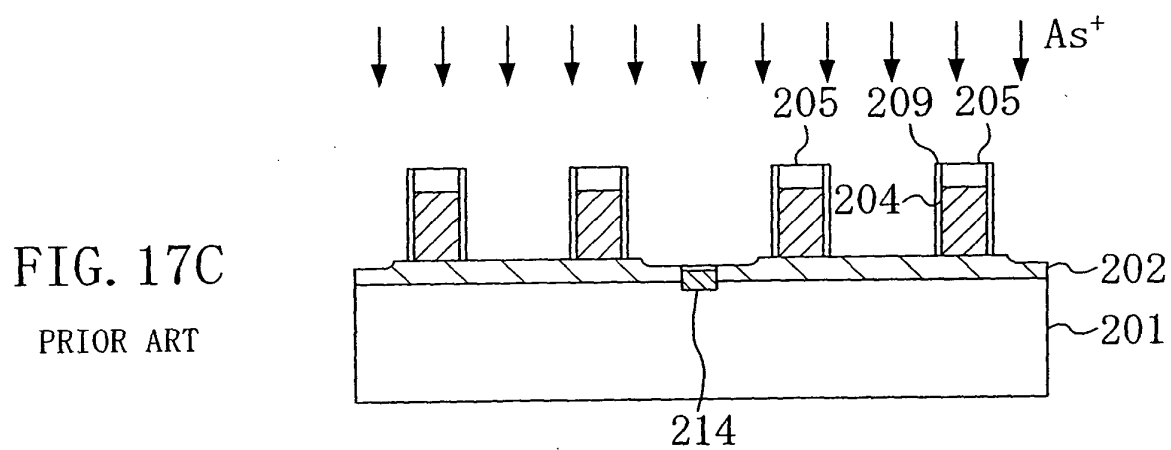
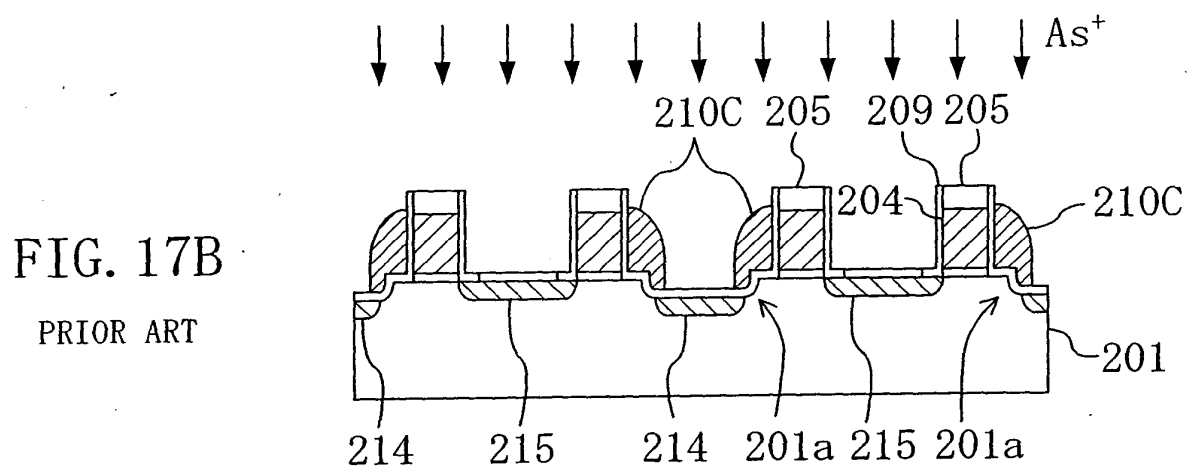
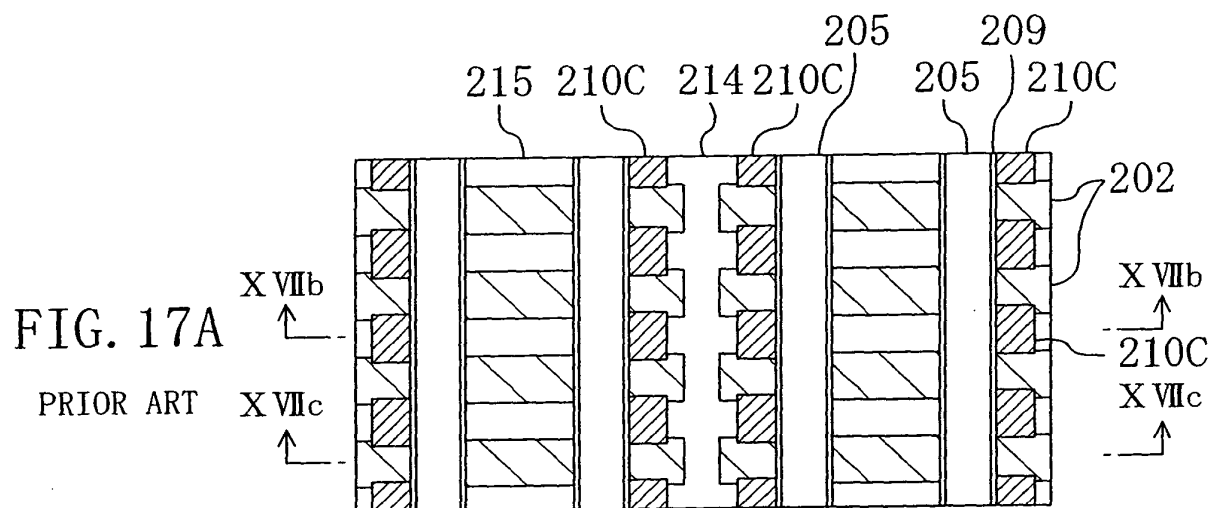


FIG. 18A

PRIOR ART

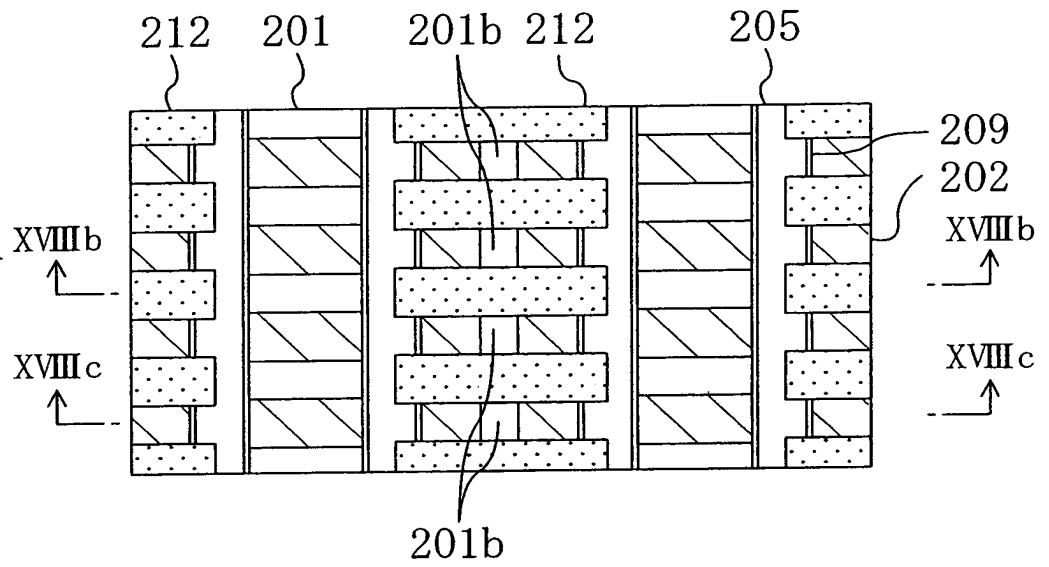


FIG. 18B

PRIOR ART

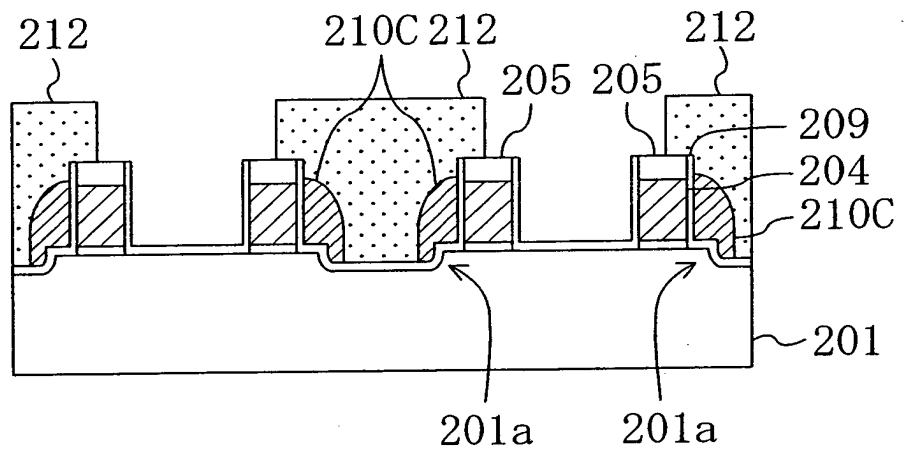


FIG. 18C

PRIOR ART

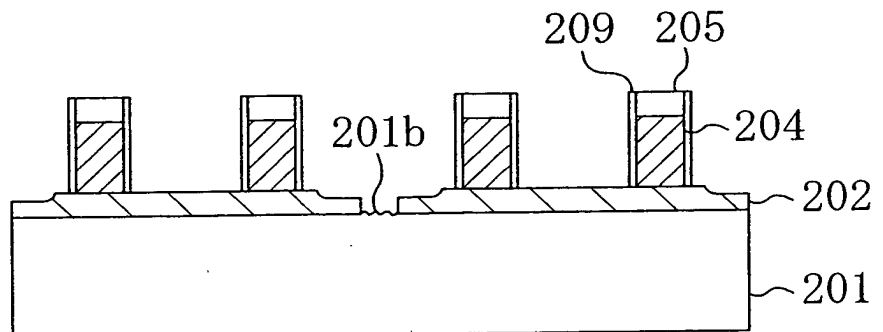


FIG. 19

PRIOR ART

